843.40811VX1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	K. SUZUKI, et al.
Application No.:	10/688,902
Filed:	October 21, 2003
For:	METHOD OF MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A PLURALITY OF WIRING LAYERS AND MASK-PATTERN GENERATION METHOD (As Amended)
Art Group of Parent:	1765
Examiner of Parent:	L. VINH

AMENDMENT

MS: AMENDMENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 26, 2005

Sir:

In response to the Office Action dated May 26, 2005, please amend the above-identified application as listed below and as set forth on the following pages:

Amendments to the Claims; and

Remarks are included following the amendments.